Examiner, as required by MPEP §§ 808.02 and 803. Even if the Examiner's assertion is true that "the product as claimed can be made by another and materially different process such as one in which the doped regions are made by an alternative doping process such as diffusion," the examination of the application in its entirety, including Groups I and II, would not pose a "serious burden" on the Examiner.

In fact, a search required for a proper examination of either Group I (claims 1-17) or II (claims 18-21) would not be significantly different from a search required for the application as a whole, due to the number of related features found in the claims of each identified Group. For example, independent claim 1 of Group I is a method claim directed to a thin film transistor including *inter alia* a substrate having an insulative surface with island-shaped layers formed on that surface. The transistor has pairs of heavily doped source/drain regions, with an impurity concentration that is higher than that of the lightly doped regions, formed outward from the lightly doped regions of the layers.

Independent claim 18 of Group II relates to an apparatus and is directed to a transistor including a substrate having an insulative surface, island-shaped layers formed on the substrate, and pairs of heavily doped source/drain regions, with an impurity concentration higher than that of the lightly doped regions, formed outward from the edges of the lightly doped regions. Claim 18 has almost identical elements as the elements in claim 1 of Group I.

Furthermore, dependent claims 8 and 13 of Group I define a transistor that has an area located in the layers including hydrogen atoms at a concentration equal to or less than

10^{17} cm^{-3} and gate insulation films having a thickness of equal to or greater than 50 nm where the gate electrodes have a thickness of equal to or greater than 200 nm, respectively. Similarly, claims 19 and 20 of Group II, define a transistor with the same hydrogen atom concentration, gate insulation film thickness, and gate electrode thickness.

Therefore, a proper search and examination of a method for manufacturing a thin film transistor having a substrate with an insulative surface, a plurality of island-shaped layers formed on the substrate, and pairs of heavily doped source/drain regions formed in the layers outward from the edges of the lightly doped regions as defined in Group I, would at least overlap and possibly fully encompass, a search and examination required for a thin film transistor having a substrate with an insulative surface, a plurality of island-shaped layers formed on the substrate, and pairs of heavily doped source/drain regions formed in the layers outward from the edges of the lightly doped regions, as recited in Group II. Accordingly, no "serious burden" would be imposed upon the Examiner by the examination of the entire application, since similar and overlapping searches are required for both of the Groups.

In view of the foregoing the applicants respectfully request that the restriction requirement be withdrawn upon reconsideration.

Respectfully submitted,
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